SYLLABUS

Discipline name	Digital Systems
Profile	Electronics and Telecommunications Engineering
Specialization	Telecommunications Technologies and Systems
Code	51322809
Course leader	Professor Sorin Hintea, Ph.D – Sorin.Hintea@bel.utcluj.ro
Collaborators	Assistant Gabor CSIPKES, Ph.D., Gabor.Csipkes@bel.utcluj.ro Assistant Robert GROZA, Robert.Groza@bel.utcluj.ro
Department	Basis of Electronics
Faculty	Electronics, Telecommunications and Information Technology

Sem.	Type of discipline	Course	Applications			Course	Applications			Ind. study	TOTAL	Credits	Form of assessment
		[hours/week]				[hours/sem.]							
			S	L	P		S	L	P				
4	**Engineering**	**2**	**-**	**1**	**1**	**28**	**-**	**14**	**14**	**94**	**150**	**5**	**Exam**

Acquired competences :

Acquired skills (what the student is able to do):

After completing the discipline, the students will be able to:
- understand the internal structure of digital circuits;
- analyze digital circuits and understand their electrical parameters;
- compensate the signal propagation and great capacities in digital circuits;
- use the digital design principles and VHDL synthesis;

Acquired abilities: (what type of equipment/instruments/software the student is able to handle)

After completing the discipline, the students will be able to:
- develop average projects that contain combinational and sequential circuits
- analyze and describe digital systems using the VHDL hardware language
- to improve the performances of the digital structures
- to use design environments for digital systems
- to avoid the logic hazard
- synthesize logic problems of various complexity

Prerequisites (if necessary)

logic functions; electronic switching circuits; analysis and synthesis of digital circuits;

A. Course/Lecture (course/lecture titles)	
1	Digital bipolar internal structures. TTL family and subdomains.
2	CMOS and NMOS digital integrated circuits. The inverter and fundamental gates .
3	Combinational and sequential circuits in CMOS VLSI technology
4	Performance analysis for CMOS circuits. Propagation times and power
5	Digital integrated VLSI circuits. Methods and examples.
6	ROM memories. Structures and internal configurations. Electrical and timing characteristics.
7	Dynamic and static RAM memories. Structures and characteristics.
8	Semiconductor memory applications. Connecting and extending the memory capacity
9	Arithmetical operations. Classical adders, subtractors and multiplying circuits in TTL and CMOS technology.
10	VLSI arithmetical circuits. Adders, subtractors and multiplying circuits in VHDL. Circuit design
11	Impulse generators. Monostables and circuits for processing the digital signals. Interface and display circuits
12	Programmable logic areas. PLA, PAL and FPGA structures
13	Computer aided design for digital circuits
14	The design of comples digital circuits. Digital VLSI circuits simulation and testing

B1. Applications – Laboratory (list of laboratories)	
1	TTL and CMOS families. Parameters and functioning.
2	Circuits with ROM and RAM memories
3	TTL and CMOS oscillators
4	Monostables and circuits for impulse processing
5	Logical hazard

SYLLABUS

6	Digital integrated circuits interface
7	Laboratory tests. Redoing of missing laboratories
Project (project contents)	
1	Structure, organizing and contents of the project; Project themes: Frewquencemeter for low frequencies, Clock dividers, Alarm clock, Taxi counter.
2	Block diagram of the project
3	Displaying types. Multiplexed and direct display.
4	Various ways of obtaining the clock signal; oscillators; programmable frequency dividers. Synchronous and asynchronous dividers.
5	Detailed design of functional blocks I.
6	Detailed design of functional blocks II.
7	Project presentation. Evaluation.

C. Individual study (reference study contents, synthesis materials, projects, applications etc.)

2 synthesis reports
6 sets of problems (the preparation part in every laboratory)
3 sets of problems (course homework)

Individual study structure	Course study	Problem solving, laboratory, project	Applications preparation	Examination time	Additional reference study	Total no. of individual study hours
Hours	28	46	7	3	10	94

References (Textbooks, courses, laboratory manual, exercise book)

1. A.E.A. Almaini. Electronic Logic Systems, Ed. Prentice Hall, 1994 (Department's library)
2. John M Yarbrough: Digital Logic. Applications and Design, West Publishing Company, 1997 (Department's library)
3. M.D. Ercegovac: Introduction to Digital Systems, Ed. JohnWiley&Sons, 1999 (Department's library)
4. J. M. Rabaey :Digital Integrated Circuits, 2nd edition, John Willey, 2002 (Department's library)
5. Marcovitz: Introduction to Logic Design, McGraw Hill, New York, 2005
6. Morris Mano, Michael Ciletti: Digital Design, Prentice Hall, SUA, 2007
7.Ben Cohen: VHDL. Coding Styles and Methodologies, an in-depth tutorial, Kluwer Academic Publishers, USA, (Department's library)

Final evaluation	
Evaluation method	Written exam (E): problem solving (80%) and theoretical subjects (20%).
Mark components	Exam (E: 0…10 points); Laboratory (L: 0…10 points); Project (P: 0…10 points);
Mark computation	M = 0.5E + 0.2L + 0.3P. Pass if: E≥4 and L≥4 and P≥4.5

Course leader,

Professor Sorin HINTEA, Ph.D.