SYLLABUS

1. Data about the program of study

1.1	Institution	The Technical University of Cluj-Napoca
1.2	Faculty	Electronics, Telecommunications and Information Technology
1.3	Department	Bases of Electronics
1.4	Field of study	Electronics and Telecommunications Engineering
1.5	Cycle of study	Bachelor of Science
1.6	Program of study/Qualification	Telecommunications Technologies and Systems/ Engineer
1.7	Form of education	Full time
1.8	Subject code	TST-E104.00

2. Data about the subject

2.1	Subject name					FPGA systems					
2.2	Subject area					Electronics and Communications Engineering					
2.3	Course responsible/lecturer					Assoc. Prof. Albert Fazakas					
2.4	Teachers in charge of applications					Assoc. Prof. Albert Fazakas					
2.5	Year of study	IV	2.6	Semester	1	2.7	Assessment	Exam	2.8	Subject category	DS/ FAC

3. Estimated total time

Year/ Sem	Subject name	No. of weeks.	Course [hours/week]	Applications [hours/week]			Course [hours/sem.]	Applications [hours/sem.]			Indiv. study.	TOTAL	Credit
				S	L	P		S	L	P			
IV/I	FPGA systems	14	2		2		28		28		48	104	4

3.1	Number of hours per week	4	3.2	of which, course	2	3.3	applications	2
3.4	Total hours in the curriculum.	56	3.5	of which, course	28	3.6	applications	28

Individual study	Hours
Manual, lecture material and notes, bibliography	12
Supplementary study in the library, online and in the field	12
Preparation for seminars/laboratory works, homework, reports, portfolios, essays	20
Tutoring	2
Exams and tests	2
Other activities	-

3.7	Total hours of individual study	48
3.8	Total hours per semester	104
3.9	Număr de credite	4

4. Pre-requisites (where appropriate)

4.1	Curriculum	Digital Integrated Circuits, Digital Systems.
4.2	Competenţe	Analysis and Design of Digital Systems Computer Aided Design for electronic circuits

5. Requirements (where appropriate)

5.1	For the course	Cluj-Napoca, Amphitheatre using video-projector
5.2	For the applications	Cluj-Napoca, Laboratory equipped with a computer network and FPGA development boards

6. Specific competences

Competențe profesionale	Theoretical knowledge (what the student must know):	Students will know and understand: – The main FPGA families and devices on the market – Aspects related to HDL (VHDL, Verilog,) coding for synthesizable and non-synthesizable codes – To interpret correctly synthesis and implementation reports in order to optimize timing and area occupied by the device – The internal structures of CPLD and FPGA devices, including special integrated components and their advantages – The FPGA and CPLD configuration and autoconfiguration methods
	Acquired skills (what the student is able to do):	After completing the discipline, the students will be able to: – Create complex digital projects using HDL description (VHDL, Verilog) – Plan and hierarchize the digital projects for partitioning and design reuse – Create testbenches, test modules, interpret waveforms from simulation and hardware debugging – Use advanced integrated components from FPGA such as BRAM, SLR, Clock PLL/DCM/MMCME – Hardware design of development systems and FPGA- or CPLD-based applications
	Acquired abilities: (what type of equipment the student is able to	After completing the discipline, the students will be able to: – Efficiently use the FPGA-specific development tools such as Xilinx ISE, Vivado Design Suite – use specific equipment for efficiently test and debug digital systems, (digital oscilloscope, logic analyzer) – use FPGA- and CPLD-based development boards – debug digital circuits on the hardware
Cross competences (Grila1 and Grila2 RNCIS)		N.A.

7. Discipline objectives (as results from the key competences gained)

7.1	General objectives	Developing competences in the analysis, design, simulation and debug of FPGA-based systems and complex digital systems
7.2	Specific objectives	1.Knowledge on the theoretical fundamentals of the analysis, modeling, design, debug or simulation of FPGA-based systems, using specific development software 2. Developing skills and abilities needed for design, implementation and debug of FPGA-based and complex digital systems 3.Developing methodologies and techniques for a systematic design that involves analytical analysis, simulation and practical experiments

8. Contents

8.1. Lecture (syllabus)		Teaching methods	Notes
1	Introduction to HDL design. Analysis of the HDL codes of the basic components	Presentation, heuristic conversation, exemplification, problem presentation, teaching exercise, case study, formative evaluation	Use of .ppt presentation, projector, blackboard
2	HDL- based design: Syntax, data types, operators and structural elements. How an HDL code is interpreted by a simulator and by a synthesizer		
3	RTL descriptions in HDL languages. Aspects of the combinational and sequential processes. Ways to avoid synthesis problems		
4	Digital systems design methodology. Verification methods: behavioral, post-translate and post-place-and route simulations.		
5	State machine types. State machine description methods. Ways to avoid hazards and increase the speed.		
6	FPGA structures. Differences from the PLA/PAL/GAL structures. Comparison between CPLD and FPGA. Base components used in FPGA structures: LUT. FF.SRL. Routing resources		
7	Xilinx FPGA families. Evolution of the families. Families of other producers (Altera, Lattice etc).		
8	Configuration methods for FPGA devices. Powering and power sequencing of FPGA devices.		
9	FPGA specific integrated components: DRAM, BRAM, IOB, Clock DLL/DCM/PLL/MMCME.		
10	The synthesis procedure. Component inference. Interpreting the synthesis reports.		
11	Aspects related to timing. Timing constraints.		
12	Generating clock signals. Clock domains. Cross-clock domain synchronization.		
13	Implementation of digital projects in FPGA devices. Place and route procedures and strategies. Methods for eliminating errors.		
14	Advanced integrated components in the FPGA devices: Serdes, XADC, DDR2/ DDR3 and MAC controllers.		
8.2. Applications (lab)		Teaching methods	Notes
1	Introduction to the ISE and Vivado design environments for Xilinx-based FPGA devices	Didactic and experimental proof, didactic exercise, team work	Use of laboratory instrumentation, experimental boards, computers, white/magnetic board.
2	Combinational circuit descriptions using HDL languages.		
3	HDL-based testbenches. Simulation using the design environments.		
4	Sequential circuit descriptions using HDL languages. Register, counter and memory description examples.		
5	Synchronous and asynchronous interconnections between components. Synchronization circuit examples. Ways to avoid hazard and metastability.		
6	FSM (Finite State Machine) design example.		
7	FSM examples for simple hardware interfaces: UART, SPI, EPP		
8	Using LUT, BRAM, SRL16, DLL/DCM/PLL/MMCME components in FPGA devices. Device instantiation examples.		
9	Importing and using pre-defied IP cores using Core Generator.		
10	Hardware debug of digital projects. Basic elements of using Hardware Manager and Chipscope.		
11	Examples for using controllers for SRAM and FLASH components.		
12	Timing analysis and timing constraints examples.		
13	FPGA configuration examples. How to create and program the external FLASH memories for autoconfiguration.		
14	Design planning by manual place and route constraints. Using constraints wizards.		

Bibliography

1. Richard E. Haskell & Darrin M. Hanna "Digital Design using Digilent FPGA Boards", 2nd Edition, LBE Books, 2012
2. Steve Kilts, "Advanced FPGA Design", John Wiley and Sons, , John Wiley and Sons, 2007

3. Albert Fazakas, Sisteme cu FPGA, notițe de curs
4. S. Hintea - Tehnologii de proiectare cu arii logice programabile, Editura UTPress, 2002
Electronic material:
1. Albert Fazakas, Sisteme cu FPGA, lucrări de laborator, http://www.bel.utcluj.ro/sfpga
2. Albert Fazakas, Sisteme cu FPGA, prezentări curs PowerPoint, http://www.bel.utcluj.ro/sfpga
3. Xilinx.inc., Free Online FPGA Design Training, http://www.xilinx.com/training/free-video-courses.htm#FPGA
4. Xilinx Products Datasheets User Guides and Application Bulletins, www.xilinx.com
5. Digilent Nexys2, Nexys3, Atlys boards reference manuals, http://www.digilentinc.com

9. Bridging course contents with the expectations of the representatives of the community, professional associations and employers in the field

Competences acquired will be used in the following COR occupations (Electronics Engineer; Telecommunications Engineer; Electronics Design Engineer; System and Computer Design Engineer; Communications Design Engineer) or in the new occupations proposed to be included in COR (Sale Support Engineer; Multimedia Applications Developer; Network Engineer; Communications Systems Test Engineer; Project Manager; Traffic Engineer; Communications Systems Consultant).

10. Evaluations

Activity type	10.1	Criterii de evaluare	10.2	Assessment methods	10.3	Weight in the final grade
Course		The level of acquired theoretical knowledge and practical skills		- Summative evaluation written exam (theory and problems)		- E, max 10 pct 50%
Applications		The level of acquired abilities		- Continuous formative evaluation - practical lab test		- L, max. 10 pct 50%
10.4 Minimum standard of performance						
L ≥ 5 and E ≥ 5 and 0.5E + 0.5L ≥ 5						

Date of filling in
12.02.2015

Course responsible
Assoc. Prof. Albert Fazakas, PhD

Teachers in charge of applications
Assoc. Prof. Albert Fazakas, PhD

Date of approval in the department
12.02.2015

Head of department
Prof. Sorin Hintea, PhD