SYLLABUS

1. Data about the program of study

1.1 Institution	Technical University of Cluj-Napoca
1.2 Faculty	Faculty of Electronics, Telecommunications and information Technology
1.3 Department	Bases of Electronics
1.4 Field of study	Electronic Engineering, Telecommunications and Information Technologies
1.5 Cycle of study	Bachelor of Science
1.6 Program of study / Qualification	Telecommunications Technologies and Systems/ Engineer
1.7 Form of education	Full time
1.8 Subject code	TST-E104.00

2. Data about the subject

2.1 Subject name	FPGA Systems						
2.2 Subject area	Theoretical area Methodological area Analytic area						
2.3 Course responsible	Assoc. Prof. Albert Fazakas – Albert.Fazakas@bel.utcluj.ro						
2.4 Teacher in charge with seminar / laboratory / project	Assoc. Prof. Albert Fazakas – Albert.Fazakas@bel.utcluj.ro						
2.5 Year of study	III	2.6 Semester	5	2.7 Assessment	E	2.8 Subject category	DS/DFac

3. Estimated total time

3.1 Number of hours per week	4	of which: 3.2 course	2	3.3 seminar / laboratory	2
3.4 To Total hours in the curriculum	56	of which: 3.5 course	28	3.6 seminar / laboratory	2

Distribution of time	hours
Manual, lecture material and notes, bibliography	18
Supplementary study in the library, online specialized platforms and in the field	18
Preparation for seminars / laboratories, homework, reports, portfolios and essays	26
Tutoring	5
Exams and tests	2
Other activities:	0

3.7 Total hours of individual study	69
3.8 Total hours per semester	125
3.9 Number of credit points	5

4. Pre-requisites (where appropriate)

4.1 curriculum	Digital Integrated Circuits, Digital Systems
4.2 competence	Analysis and Design of Digital Systems CAD tools for analysis and design of Digital Systems

5. Requirements (where appropriate)

5.1. for the course	Cluj-Napoca, classroom equipped with video projector
5.2. for the seminars / laboratories / projects	Cluj-Napoca, classroom equipped with computer network, Vivado Design System software, 7-Series and Zynq-based FPGA development systems, specific peripheral modules

6. Specific competences

Professional competences	N/A
Transversal competences	N/A

7. Discipline objectives (as results from the key competences gained)

7.1 General objective	Professional skill development in the field of FPGA/SoC-based Digital Systems Design, using HDL description languages and reconfigurable microprocessor systems
7.2 Specific objectives	1. Theoretical knowledge of FPGA/SoC structures, understanding their possibilities and limitations 2. Knowledge of specific CAD software tools for FPGA - and SoC – based systems 3. Knowledge of Hardware Description Languages and their efficient usage for Digital Design creation 4. Developing skills for testing, debug and optimization of digital projects for speed and/or area 5. Gaining knowledge of how to use the FPGA-specific digital components efficiently: BRAM, DDR controllers, Clocking Circuits etc. 6. Developing systematic design and methodologies that combine analysis simulation and practical experiments

8. Contents

8.1 Lecture (syllabus)	Teaching methods	Notes
1. Introduction. What is FPGA? State-of-the Art in FPGA – and SoC- based systems and development tools.	Presentation, heuristic conversation, exemplification, problem presentation and solving, case studies	Video projector and blackboard are used
2. Microblaze microprocessor systems in 7-series FPGAs. ARM-based systems in ZynQ – based architectures. The AMBA bus concept. The AXI bus.		
3. Software access for AXI-based peripherals Low-Level access. Driver-based access.		
4. Interrupt controllers and interrupts in Microblaze and ARM-based systems.		
5. Real-time process control. Using timer and interrupts.		

6. FPGA Design methodology. Design Entry, Synthesis and Implementation. Project Verification methods.		
7. The AXI-Lite protocol. Processor-peripheral communication model and handshake. Adding user peripherals to a microprocessor-based system.		
8. User IP core HDL structure. Port and parameter propagation and through the peripheral architecture.		
9. Synthesis of digital circuits. Design optimization techniques used by the synthesizer. FSM types and description techniques		
10. Hazard in digital circuits and hazard avoiding techniques. High-speed design techniques. Specific digital design techniques: pipelining, register replication. Synchronous design techniques		
11. FPGA configuration methods. The JTAG controller. Configuration sequence from power-up to EOS. Partial reconfiguration.		
12. FGA powering. Power supply lines and decoupling, Power sequencing. Power supply and temperature monitoring: the XADC primitive.		
13. FPGA clocking. Clock signal distribution: Global and regional clocks. Components for clock synthesis. Design constraints for clock synthesis		
14. Synthesis of digital circuits using High-Level Synthesis – HLS language		

Bibliography

1. Albert Fazakas, Sisteme cu FPGA, prezentări PowerPoint, 2018-2019
2. Steve Kilts, ”Advanced FPGA Design”, John Wiley and Sons, 2007
3. Xilinx inc., „Artix-7 FPGAs Data Sheet: Overview”, DS180 (v2.6) February 27, 2018, www.xilinx.com
   - Datasheets and User Guides for the 7-Series FPGA: DS181, UG470...UG476
4. Xilinx inc., „Zynq-7000 SoC Data Sheet: Overview”, DS190 (v1.11.1) July 2, 2018, www.xilinx.com
   - Datasheets and User Guides for the 7-Series ZynQ SoC, : UG585, DS191, DS187, UG1165, UG873

8.2 Laboratory	Teaching methods	Notes
1. Introduction Familiarizing with the Xilinx Vivado Design Environment and the Digilent Nexys4DDR and Zybo development boards.	Practical experiment and proof of concepts, teamwork	FPGA- and SoC-based boards, laboratory equipment, Vivado software, video projector and blackboard are used.
2. Accessing peripheral registries at low-level. Program debugging using hardware and software debug tools. Analyzing signals using logic analyzer.		
3. Accessing peripherals by device drivers. Microblaze and ARM-9 examples.		
4. Adding new peripherals to a processor system. Adding and connecting interrupt controller and timers. Software configuration of the newly added peripherals		
5. Configuring and enabling interrupt routines. Examples for process control.		
6. Simulating Microblaze-based projects. The AXI Lite protocol. Peripheral register access.		

7. Synchronizing external signals to the system clock. Debouncing and synchronization circuits		
8. Creating a custom IP core I. Connecting and checking HDL blocks to the peripheral AXI attachment. Connecting to the user registers.		
9. Creating a custom IP core II. Software application.		
10. Clock signal generation. The MMCM2E_ADV and PLL2E_ADV primitives. Example: VGA interface for different resolutions.		
11. Timing constraints. Example for creating and editing timing constraints.		
12. VGA interface for Microblaze and ARM systems. The Video DMA (VDMA) component.		
13. Project hardware debugging. Accessing internal signals. The Integrated Logic Analyzer (ILA) and Virtual I/O (VIO) cores.		
14. FPGA configuration examples. External FLASH memory configuration file creation. Programming external configuration FLASH.		

Bibliography

1. Albert Fazakas, Sisteme cu FPGA, lucrări de laborator, 2018-2019
2. Digilent inc., „Nexys4DDR User Manual", rev. C, April 11, 2016, https://reference.digilentinc.com/_media/nexys4-ddr:nexys4ddr_rm.pdf
3. Digilent inc., „Nexys4DDR Schematics", rev. C, 2014, https://reference.digilentinc.com/_media/nexys4-ddr:nexys_4_ddr_sch.pdf
4. Digilent inc., „Zybo Z7 Board Reference Manual", Revised February 21, 2018, https://reference.digilentinc.com/_media/reference/programmable-logic/zybo-z7/zybo-z7_rm.pdf
5. Digilent inc., „Zybo Z7 Board Schematic", Rev. B.2, Copyright 2017, https://reference.digilentinc.com/_media/reference/programmable-logic/zybo-z7/zybo_z7_sch-public.pdf
6. Xilinx inc., „Vivado Design Suite User Guide: Getting Started", UG910, https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_4/ug910-vivado-getting-started.pdf
7. Xilinx inc., „Vivado Design Suite User Guide: Using the Vivado IDE", UG893, https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_4/ug893-vivado-ide.pdf

9. Bridging course contents with the expectations of the representatives of the community, professional associations and employers in the field

The discipline content and the acquired skills are in agreement with the expectations of the professional organizations and the employers in the field, where the students carry out the internship stages and/or occupy a job (in the field of digital system design, simulation and testing), and the expectations of the national organization for quality assurance (ARACIS).

10. Evaluation

Activity type	10.1 Assessment criteria	10.2 Assessment methods	10.3 Weight in the final grade
10.4 Course	The level of acquired theoretical knowledge and practical skills	C – Formative in-presentation evaluation	C (max. 1 p)

		(answer to the questions asked by the teacher) WE – Written exam for overall evaluation (solving problems)	WE (max. 10 pct.), 40%
10.5 Seminar/ Laboratory	The level of acquired knowledge and abilities	LR – 4 Laboratory Reports (solving Laboratory Exercises) P – Practical project implemented on FPGA or SoC development board, using specific CAD tools	LR1, LR2, LR3, LR4 (max. 10p) - P (max. 10 pct.), 60%
10.6 Minimum standard of performance			
Quality aspects: Minimal knowledge level: ✓ Knowledge about the FPGA and SoC principle, specific CAD tools, hardware and software design creation ✓ Project verification and debugging **Quantity aspects:** ✓ Passing all the Laboratory Works and obtaining passing grade on all the Laboratory Reports (LR) ✓ Passing the Project (P) and Written Exam (WE), minimal grade: 5 ✓ Final grade formula: = 0.4WE + 0.6P + C			

Date of filling in:	**Responsible**	**Title Surname NAME**	**Signature**
27.09.2021	Course	Assoc. Prof. Albert FAZAKAS, PhD	
	Applications	Assoc. Prof. Albert FAZAKAS, PhD	

Date of approval in the Department of Communications 27.09.2021	Head of Communications Department Prof. Virgil DOBROTA, Ph.D.
Date of approval in the Council of Faculty of Electronics, Telecommunications and Information Technology 27.09.2021	Dean Prof. Gabriel OLTEAN, Ph.D.